AMENDMENTS TO THE CLAIMS

Without prejudice, this listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Currently Amended) A method for monitoring a microprocessor using an assigned watchdog, comprising:

causing the watchdog to monitor a reception of a reset pulse within a time interval of a predetermined duration;

causing the watchdog to initiate a reset of the microprocessor if the reset pulse is not received; and

executing at least one check function of the watchdog in an operating phase of the microprocessor, each one of the at least one check function including a reset of the watchdog and an execution of a sequence of waiting loops, wherein a duration of the execution of the sequence of waiting loops of at least one of the at least one check function is greater than the predetermined duration of the time interval;

incrementing a counter with the execution of the at least one check function, the execution of the at least one check function being a function of a content of the counter;

wherein:

the counter has four counter contents,

an analysis is performed at one of the four counter contents, and

the least one check function is executed each time at the other counter contents.

2. (Original) The method as recited in Claim 1, further comprising:

generating an error message if the watchdog has not reset the microprocessor by an end of the sequence of waiting loops.

3. (Canceled).

4. (Currently Amended) The method as recited in Claim [[3]] 1, further comprising:

performing the at least one check function at the content of the counter; and

skipping the at least one check function at another content of the counter, the counter alternating between the content of the counter and the other content of the counter.

5. (Canceled).

6. (Original) The method as recited in Claim 5, wherein:

a variable of the at least one check function corresponding to the duration of the sequence of waiting loops, is changed as a function of the counter content by changing a number of waiting loops contained in the sequence.

7. (Currently Amended) The method as recited in Claim [[6]] 1, wherein:

the duration of the sequence of waiting loops is reduced with each subsequent execution of the at least one check function, the duration being less than the time interval of the watchdog during the last execution, before the at least one check function is skipped.

8. (Currently Amended) The method as recited in Claim 1, wherein:

a number of waiting loops in the sequence of waiting loops is selected during at least one execution of the at least one check function ~~in such a way that the duration of the execution of the sequence of waiting loops is less than the time interval gives a clock rate that is slightly above an upper tolerance limit~~ so that the duration of the execution is below the time interval if the clock rate is slightly above the upper tolerance limit.

9. The method as recited in Claim 1, wherein:

the operating phase is at least a switching on of the microprocessor.

10. (Original) The method as recited in Claim 1, wherein:

the watchdog is supplied a clock signal that differs from a clock signal of the microprocessor.

11. (Currently Amended) A circuit arrangement, comprising:

a counter;

a microprocessor;

a watchdog assigned to the microprocessor and for performing a reset of the microprocessor if a reset pulse is not received within a time interval of predetermined duration, wherein:

a different clock signal is supplied to the watchdog than to the microprocessor; and

a non-volatile memory to which is assigned the microprocessor, at least a counter content of the counter being stored in the non-volatile memory;

wherein the counter is incremented with the execution of the at least one check function, the execution of the at least one check function being a function of a content of the counter, and

wherein:

the counter has a plurality of counter contents,

an analysis is performed at one of the plurality of counter contents, and

the least one check function is executed each time at the other counter contents.

12. (Original) The circuit arrangement as recited in Claim 11, wherein:

the non-volatile memory includes an EEPROM.

13. (Original) The circuit arrangement as recited in Claim 11, wherein:

the non-volatile memory is a part of the microprocessor.

14. (Currently Amended) A memory component storing a computer program that when executed on a microprocessor results in a performance of the following:

causing a watchdog to monitor a reception of a reset pulse within a time interval of a predetermined duration;

causing the watchdog to initiate a reset of the microprocessor if the reset pulse is not received; and

executing at least one check function of the watchdog in an operating phase of the microprocessor, each one of the at least one check function including a reset of the watchdog and an execution of a sequence of waiting loops, wherein a duration of the execution of the sequence of waiting loops of at least one of the at least one check function is greater than the predetermined duration of the time interval;

incrementing a counter with the execution of the at least one check function, the execution of the at least one check function being a function of a content of the counter;

wherein:

the counter has a plurality of counter contents,

an analysis is performed at one of the plurality of counter contents, and the least one check function is executed each time at the other counter contents.